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(71) Applicant : **WESTINGHOUSE ELECTRIC CORPORATION**
Westinghouse Building
Gateway Center
Pittsburgh Pennsylvania 15222 (US)

(72) Inventor : **Mackenzie, Raymond Warren**
3837 Cynthia Drive
Pittsburg, PA 15227 (US)
Inventor : **Engel, Joseph Charles**
107 Overlook Circle
Monroeville, PA 15146 (US)

(74) Representative : **van Berlyn, Ronald Gilbert et al**
23, Centre Heights
London NW3 6JG (GB)

(54) Circuit breaker responsive to repeated in-rush currents produced by a sputtering arc fault.

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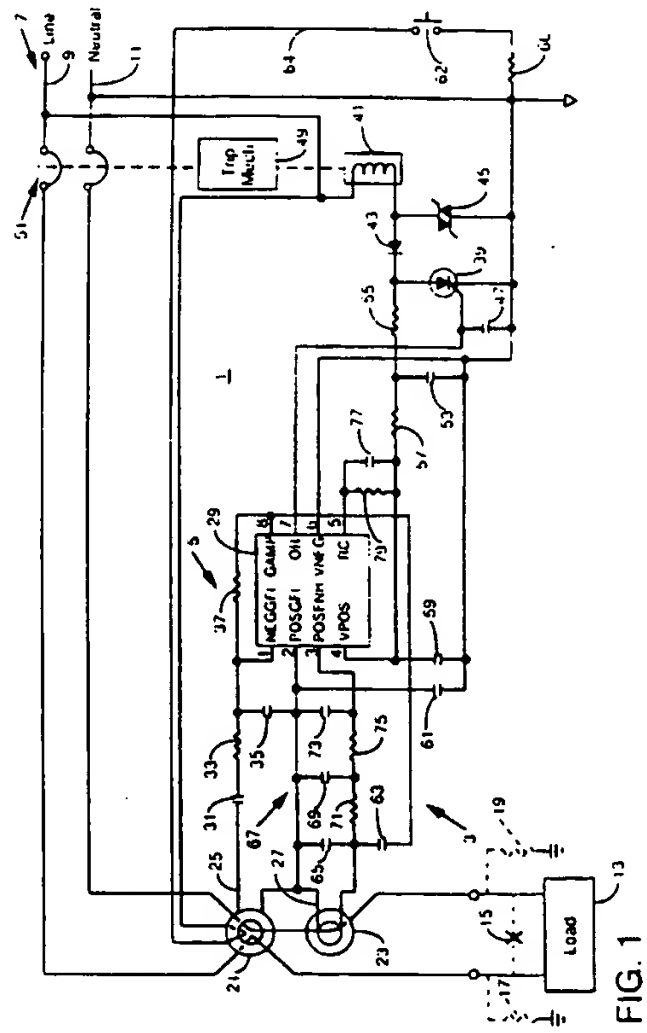

FIG. 1

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described in U.S. patent no. 4,081,852 which is herein incorporated by reference. That circuit breaker includes a thermo-magnetic overcurrent trip mechanism and a ground fault detector mounted in side-by-side compartments within a molded housing. The ground fault detector includes a trip solenoid having a plunger which extends through the wall between the two compartments in the molded housing to actuate the thermo-magnetic trip mechanism to trip the circuit breaker in response to a ground fault.

As shown in Figure 1, the circuit breaker 1 of the invention, in its preferred embodiment, combines a sputtering arc detector 3 with a ground fault detector 5. The circuit breaker 1 protects an electric system 7 which includes a line conductor 9 and a neutral conductor 11 which provide electric power to a load 13. In addition to protecting against typical overcurrents drawn by the load 13 and bolted line-to-neutral faults, the circuit breaker 1 of the invention protects against sputtering arc faults 15 between the line conductor 9 and a neutral conductor 11, and line-to-ground faults 17 and neutral-to-ground faults 19. As discussed above, the sputtering arc fault 15 results when bared sections of the line and neutral conductors come in contact due to, for instance, worn or stripped insulation.

Faults in the electrical system 7 are detected by the circuit breaker 1 by current sensors in the form of current transformers 21 and 23. These current transformers 21 and 23 are toroidal coils. The line conductor 9 and neutral conductor 11 are passed through the opening in the toroidal coil 21 to form the primary of that current transformer. The current transformer 23 has a single primary in the form of the neutral conductor 11 which passes through the opening of the toroidal coil. The second winding 25 of the current transformer 21 and the second winding 27 of the current transformer 23 are each connected to an integrated circuit 29.

The current transformer 21 detects line-to-ground faults. With no line-to-ground fault on the electrical system 7, the currents through the line and neutral conductors 9, 11 which form the primaries of the transformer will be equal and opposite so that no current will be induced in the secondary winding 25. If the line conductor 9 is grounded, there will be a large current through this conductor and little or no current through the neutral conductor 11 so that a sizable current will be induced in the secondary winding 25. This signal is applied to the IC 29 through the NEGGFI and POSGFI inputs through a dc blocking capacitor 31 so that offsets in an op amp (to be described) in the IC are not applied to the current transformer 21. A resistor 33 critically dampens resonance caused by the series connected capacitor 31 and secondary winding 25 of the current transformer 21. A capacitor 35 across the IC inputs provides noise suppression. A feedback resistor 37 sets the gain for the op amp in the IC 29.

As will be discussed in more detail below, if the magnitude of the current in the secondary winding 25 of the current transformer 21 exceeds a threshold selected to detect a line-to-ground fault, the OR output on the IC 29 goes high to turn on an SCR 39. Turning on of the SCR 39 provides current for energization of a trip solenoid 41 with current drawn from the line and neutral conductors. This current is half wave rectified by the diode 43. The SCR 39 is protected from surges by the metal oxide varistor (MOV) 45 and from noise on the gate by capacitor 47. Energization of the trip solenoid 41 actuates the trip mechanism 49 as described in U.S. patent no. 4,081,852 to open contacts 51 at least in the line conductor 9, and preferably also in the neutral conductor 11.

The diode 43 also provides DC power to a shunt regulator in the IC 29. The current drawn by the IC is insufficient to actuate the trip solenoid 41. The power supply for the IC 29 includes a filter capacitor 53, and a pair of resistors 55 and 57 which determine the voltage level of the supply. This DC power is provided to the VPOS input of the IC 29. The VNEG pin is connected to the ground for the neutral conductor. A bypass capacitor 59 assures that there is no ac on the VPOS input. Similarly, another bypass capacitor 61 eliminates ac on the POSGFI input.

The ground fault detector 5 is of the dormant oscillator type. The secondary winding 27 of the current transformer 23 is also connected to the output of the op amp in the IC 29 at pin GANP through a coupling capacitor 63. Neutral-to-ground faults couple the secondary windings 25 and 27 though the current transformers 21 and 23 to form a feedback loop around the IC 29 causing the op amp in the IC to oscillate. The frequency of this oscillation can be set by the selection of the value of the capacitor 63 and the capacitor 65 as well as the parameters of the current transformers 21 and 23. In the exemplary circuit breaker, this frequency is about 20 KHz. When the magnitude of the oscillation exceeds selected thresholds, the SCR 39 is fired to trip the circuit breaker.

In accordance with the invention, the current transformer 23 is also used to sense current for detecting sputtering arc faults. The rate of change of current signal, di/dt, needed for sputtering arc fault detection, is generated by providing a core in the current transformer 23 which does not saturate at the current level required to produce a trip. A suitable material for the core is powdered iron which has a low mu and a high flux saturation level. Such a core only affects the neutral ground detection by increasing the frequency of oscillation by a small amount.

The di/dt signal produced on the secondary winding 27 of the current transformer 23 is bandwidth with limited by passing it through a low pass filter 67. This is a two pole low pass filter with the first pole formed by the capacitor 69 and resistor 71, and the second

pole formed by the capacitor 73 and resistor 75. This low pass filter 67 in the exemplary circuit breaker has a half-power point at about 2 KHz. As discussed in the above referenced patent application, the di/dt signal can be used to provide an indication of overcurrent, line-to-neutral faults and sputtering arc faults. The parameters of the bandwidth limiting low pass filter 67 are selected to attenuate the spikes in the di/dt signal caused by a sputtering arc fault, and to regulate the relative sensitivity of the circuit to the sinusoidal currents of the overcurrent line-to-neutral faults and step functions of the sputtering arc faults. As also discussed above, the present invention distinguishes sputtering arc faults from the in-rush currents caused by some appliances by counting the number of step functions detected within a predetermined time period. A capacitor 77 and resistor 79 set the selected time interval in the manner to be discussed below.

Figure 2 is a schematic circuit diagram of the IC 29. The chip 29 has a power supply 81 which is energized by the half wave rectified supply described above through the VPOS and VNEG pins. An op amp 83 amplifies the signal on the secondary of the current transformer 21 for application to a window comparator 85 comprising the comparators 87 and 89. The comparator 87 is biased by a reference voltage provided by the power supply 81 which is the positive threshold for detecting line-to-ground faults. Similarly, a negative threshold bias voltage is applied to the comparator 89. A bias voltage, which is roughly the midpoint of the power supply voltage, is applied to the noninverting input of the op amp 83. A pull-up resistor 91 is connected between the outputs of the comparators 87 and 89 and VPOS. The output of these comparators is also connected to an inverting input of an OR circuit 93, the output of which is connected to the gate of the SCR 39 through the OR pin of the IC 29. Normally, the outputs of the comparators 87 and 89 are high so that the SCR 39 is not gated. The presence of a line-to-ground fault causes a signal generated on the secondary winding 25 of the current transformer 21 to exceed the thresholds applied to the comparators 87 and 89 during alternate half cycles of the load current. Positive half cycles of the ground fault current cause the output of comparator 87 to go low so that the output of the OR circuit 93 goes high to gate the SCR 39 and energize the trip solenoid 41. On negative half cycles, the comparator 89 turns on the SCR 39.

As previously discussed, for neutral-to-ground faults, the second current transformer 23 is connected to the output of the op amp 83 through coupling capacitor 63 connected to the GANP pin of the IC 29. Any neutral-to-ground fault completes a feedback loop between the current transformer 23 connected to the output of the op amp 83 and the current transformer 21 connected to the input. When the magnitude of this oscillation exceeds the thresholds of the window comparator 85, the SCR 39 is gated through the OR 93.

As mentioned, the current transformer 23 is also used to detect sputtering arc faults. The di/dt signal generated on the secondary winding 27, which is bandwidth limited by the low pass filter 67, is applied to a follower op amp 95 to a second window comparator 97 comprising the comparators 99 and 101. The comparators 99 and 101 compare the bandwidth limited di/dt signal to positive and negative thresholds set by the power supply 81. A pull-up resistor 103 connected to VPOS maintains a high logic signal at the outputs of the comparators 99 and 101 when the bandwidth limited di/dt signal is within the selected limits. When a current wave form representative of a sputtering arc fault is detected, the output of the window comparator 97 goes low. As certain appliances can generate a similar wave form, albeit typically of lower magnitude, a counter circuit 107 is provided on the output of the window comparator 97. The counter circuit 107 counts events in which the thresholds of the window comparator 97 are exceeded. In the preferred embodiment of the invention, the counting circuit 107 generates a trip signal on the occurrence of two such events within the selected time interval.

The counter circuit 107 includes a D flip-flop 109. The flip-flop 109 is clocked by the output of the window comparator 97 through an inverter 111. The output of the window comparator 97 is also connected through a diode 113 to the inverting input of a comparator 115. This comparator 115 compares the output of the window comparator 97 with the positive threshold voltage generated by the power supply 81. Typically, this reference voltage is about three-quarters of the power supply voltage. The output of the comparator 115 is applied to the data input D of the flip-flop 109. The $\overline{Q}$ output of the flip-flop 109, which is not used in the circuit of Figure 2, goes to the logic value of the signal at the D terminal when a clock pulse is applied to the CLK input. Thus, the $\overline{Q}$ output of the flip-flop goes to the logical opposite of the signal applied to the D input when the flip-flop is clocked. The $\overline{Q}$ is connected to an inverting input of the OR 93.

The inverting input of the comparator 115 is also connected through the RC pin of the IC 29 to the timing capacitor 77 (see figure 1). The other side of the capacitor 77 is connected to VPOS. Under normal circumstances, the capacitor 77 is discharged by the shunt resistor 79. Therefore, the output of the comparator 115 is low. When the output of the window comparator 97 goes low for the first time, indicating a sputtering arc fault event, the flip-flop 109 is clocked by the leading edge of the pulse. As the D input was low at the time of the clock pulse, the $\overline{Q}$ output remains high, and no gate signal is applied to the SCR

39 through the OR 93. When the output of the window comparator 97 goes low, the capacitor 77 charges rapidly through the diode 113 to approximately VPOS. As the voltage on the noninverting input now exceeds the reference voltage, the output of the comparator 115 goes high. When the output of the window comparator 97 again goes high as the sputtering arc current reaches its peak magnitude, the capacitor 77 begins to discharge through the resistor 79. The values of these components are selected so that the voltage on the capacitor 77 remains above the reference voltage applied to the comparator 115 for the selected time interval. As mentioned, a suitable time interval is about one second. If the output of the window comparator 97 goes low before the timer has timed out, which is indicative of a sputtering arc fault, the D input of the flip-flop 109 will be high when the flip-flop is clocked, and hence the $\overline{Q}$ output will go low, causing the output of OR 93 to go high and gate the SCR 39 on to energize the trip solenoid 41.

The sputtering arc fault detector 3' can be used independently of ground fault detection. In that case, the line conductor 9, rather than the neutral conductor 11, would pass through the core of a current transformer 23. Also, if the sputtering arc fault detection is to be provided independent of ground fault protection, the resistance of the neutral conductor could be used to detect sputtering arc faults. Figure 3 illustrates a portion of the circuit breaker 1 with the sputtering arc fault detector 3' so modified. As shown, the resistivity 117 of the neutral conductor 11 generates a voltage which is passed through a low pass filter 119 comprising the resistor 121 and capacitor 123. The output of this low pass filter is then differentiated by a highpass filter 125 comprising a capacitor 127 and resistor 129. This combination of a low pass filter 119 followed by a high pass filter 125 produces the same bandwidth limited di/dt signal as the coil circuit of Figure 1, although at a significantly lower signal level. As in the case of the circuit breaker of Figure 1, the bandwidth limited di/dt signal is applied to the noninverting input of the follower amplifier 95. The remainder of the sputtering arc detector circuit 3' is the same as shown in Figure 1.

Other variations of the sputtering arc fault responsive circuit breaker 1 are possible. For instance, in place of the window comparators 85 and 97, single comparators can be preceded by full wave rectifiers. Also, other counter circuits to count the sputtering arc fault events could be used. One variation with a higher pin count, but with no digital devices, and therefore possibly a higher noise immunity, utilizes a storage capacitor along with an additional R-C network and simple gating means. The storage capacitor is charged by the level detection means, and the capacitor terminal is also connected to one of two gate inputs via the R-C delay network. The output of level detection means is also directly applied to the second gate input, so that two outputs of the level detection means are required to produce a gate output.

Another possibility for the counter circuit is a monostable multi-vibrator, which would produce a constant width output pulse in response to the input from the level detection means. The constant width output pulses would be integrated and level detected to provide a trip on the second (or any other desired) pulse.

The improved circuit breaker of the invention, which trips on the second pulse generated by a sputtering arc fault, provides improved discrimination between arcing wiring and appliance turn-on. The improvement allows the sensing level to therefore be set much lower than otherwise would be possible.

While specific embodiments of the invention have been described in detail, it will be appreciated by those skilled in the art that various modifications and alternatives to those details could be developed in light of the overall teachings of the disclosure. Accordingly, the particular arrangements disclosed are meant to be illustrative only and not limiting as to the scope of the invention which is to be given the full breadth of the appended claims and any and all equivalents thereof.

Claims

1. A circuit breaker for protecting an ac electrical system from sputtering arc faults, characterized by a current sensing device sensing current flowing in said electrical system, an event generating device responsive to said current sensing means generating a bandwidth limited rate of change of current (di/dt) signal, a trip signal device generating a trip signal in response to a plurality of event signals within a preselected time interval; and interrupting device responsive to said trip signal interrupting current flowing in said electrical system.

2. The circuit breaker of claim 1 wherein said trip signal device generates the trip signal in response to two event signals within said preselected time interval.

3. The circuit breaker of claim 2 wherein said trip signal device generates a trip signal in response to two event signals within about a one second time interval.

4. The circuit breaker of claim 1 wherein said trip signal device comprises a counter counting said event signals.

5. The circuit breaker of claim 1 wherein said event

generating device includes a bandwidth device comparing said bandwidth limited di/dt signal to threshold values and generating the event signal when said threshold values are exceeded.

6. The circuit breaker of claim 5 wherein said trip signal device comprises a counter counting said event signals and a timer timing the selected interval.

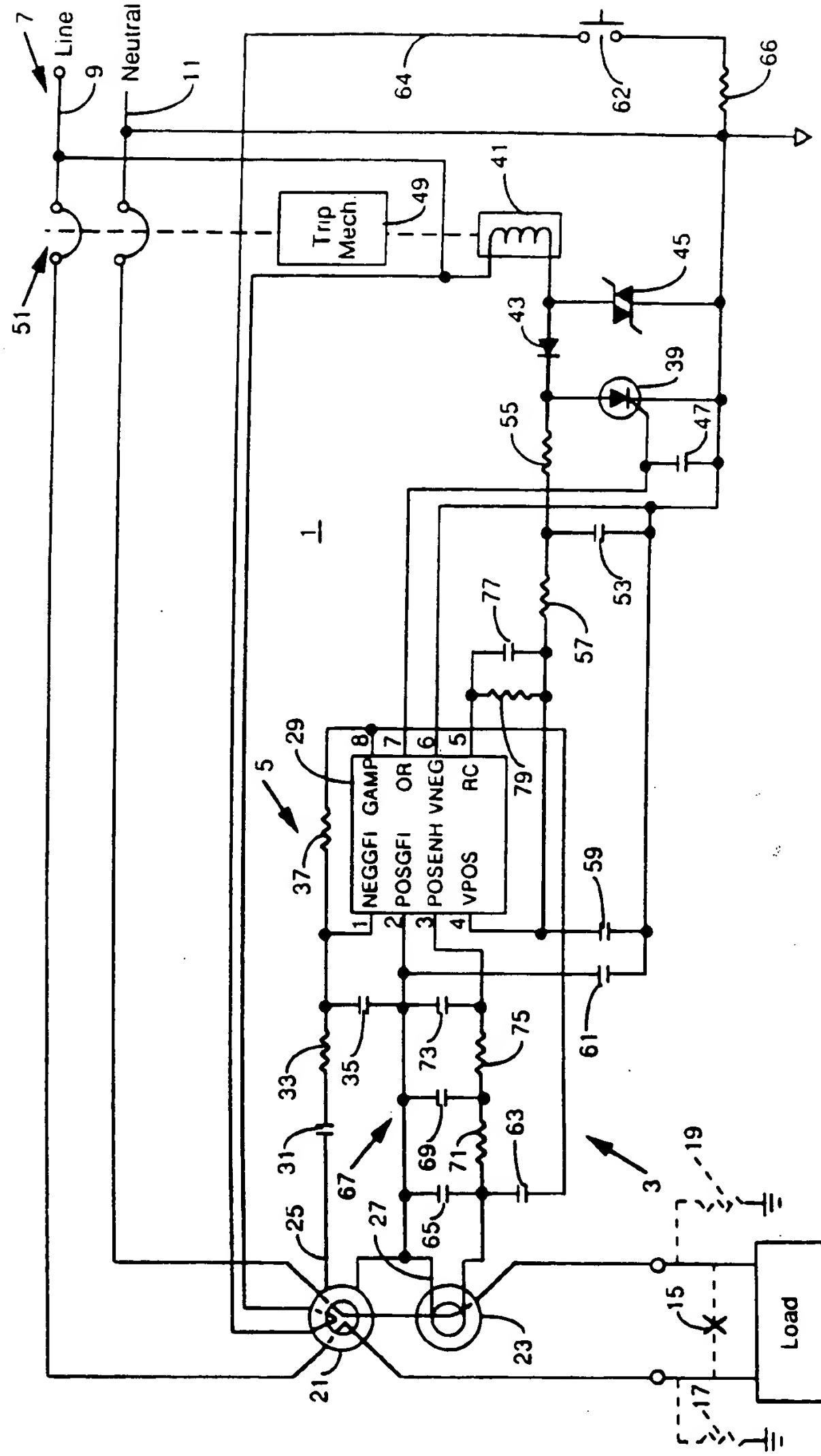
7. The circuit breaker of claim 6 wherein said counter generates said trip signal when two event signals are generated within said predetermined time interval.

8. The circuit breaker of claim 7 wherein said timer generates a timing interval of approximately one second.

9. The circuit breaker of claim 5 wherein said current sensing device comprises a signal generating device generating a di/dt signal and said event generating device generating said bandwidth limited di/dt signal comprises a two pole, low pass filter.

10. The circuit breaker of claim 5 wherein said current sensing device includes a resistivity device connected across a portion of a conductor within said circuit breaker carrying current of said electrical system to utilize resistivity of said portion of said conductor to detect current, and a bandwidth limited signal generating device for generating said bandwidth limited di/dt signal from the current detected.

11. The circuit breaker of claim 10 wherein said bandwidth limited signal genrating device comprises a low pass filter followed by a high pass filter.


7
Line
9
Neutral
11
64
62
66
51
Trip Mech.
49
41
45
43
39
55
47
1
53
77
57
29
5
NEGGFI
GAMP
POSGFI
OR
POSENH
VNEG
VPOS
RC
79
37
59
61
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67
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71
63
3
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25
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65
23
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15
Load
13
17

FIG. 1

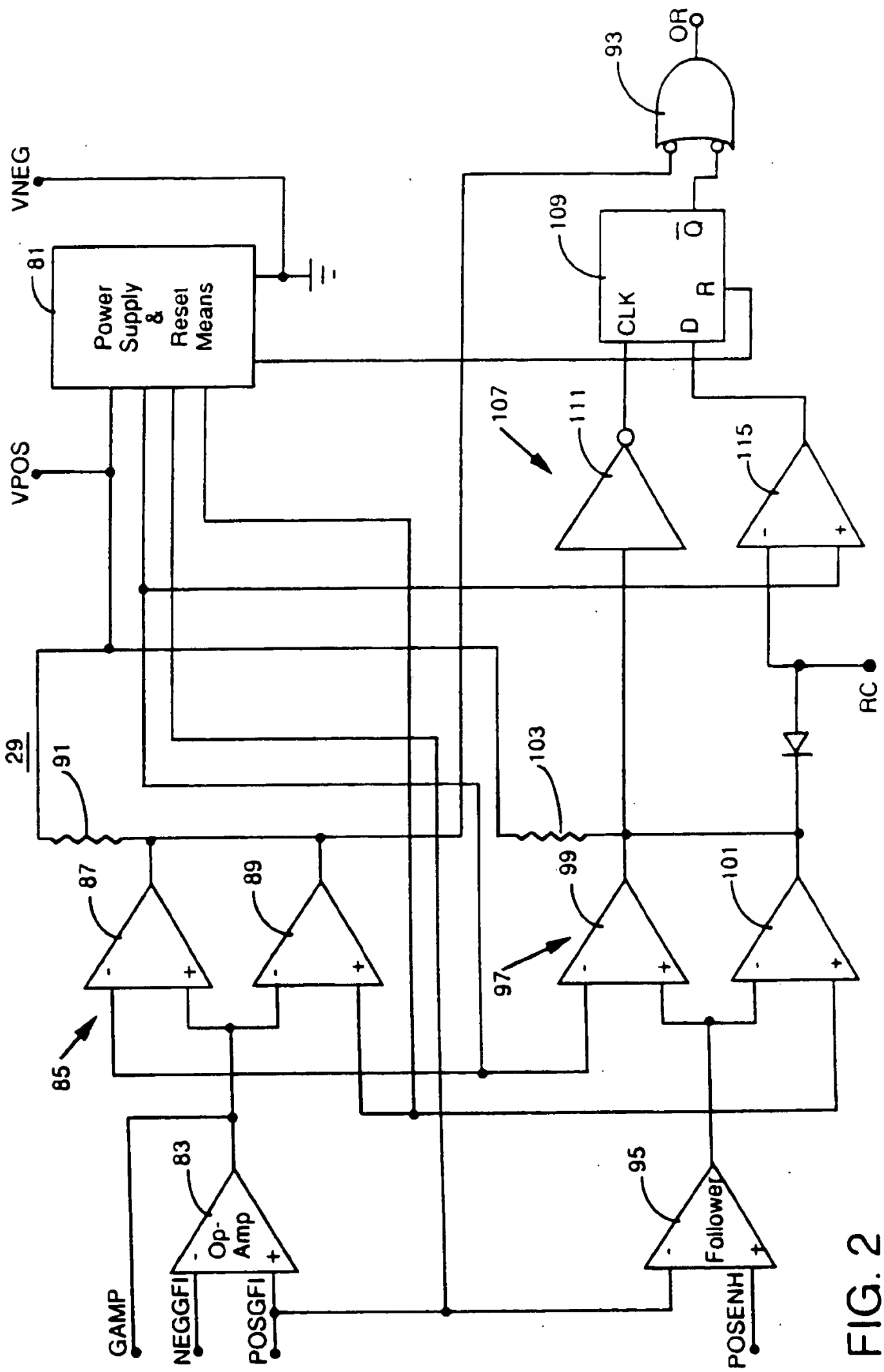
VNEG
VPOS
81
Power Supply & Reset Means
93
OR
109
CLK
D
R
Q
107
111
115
RC
29
91
103
87
89
99
101
97
85
83
Op-Amp
95
Follower
GAMP
NEGGFI
POSGFI
POSENH

FIG. 2

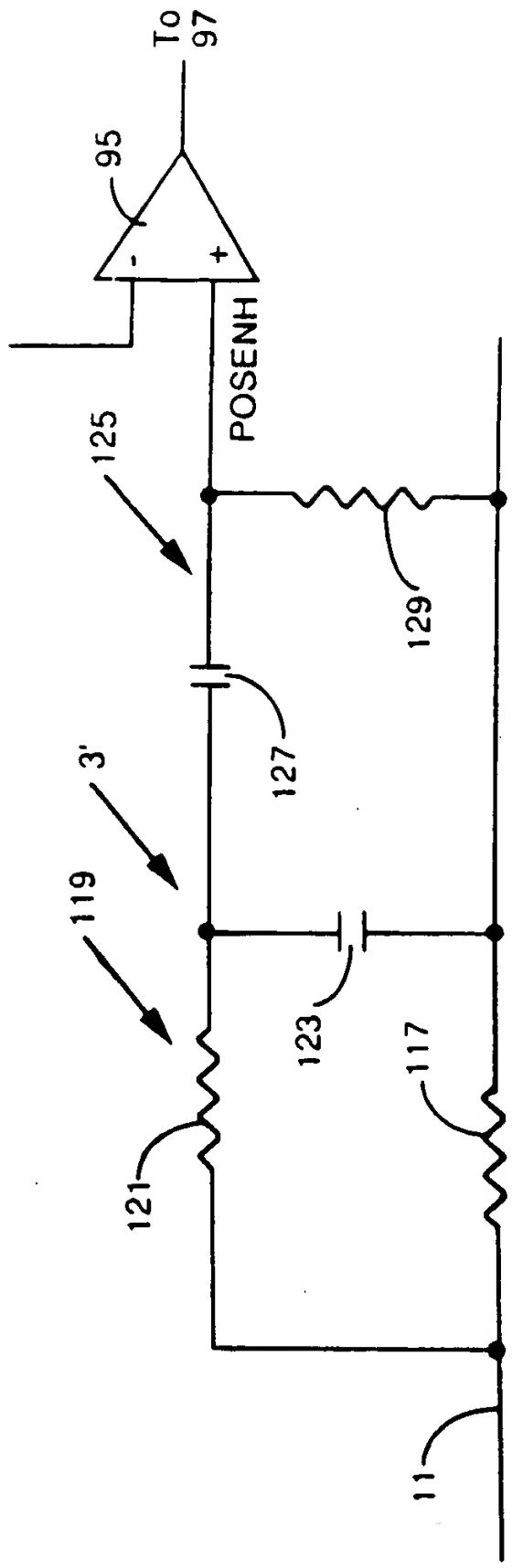

FIG. 3

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(71) Applicant : **WESTINGHOUSE ELECTRIC CORPORATION**
Westinghouse Building
Gateway Center
Pittsburgh Pennsylvania 15222 (US)

(72) Inventor : **Mackenzie, Raymond Warren**
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Pittsburg, PA 15227 (US)
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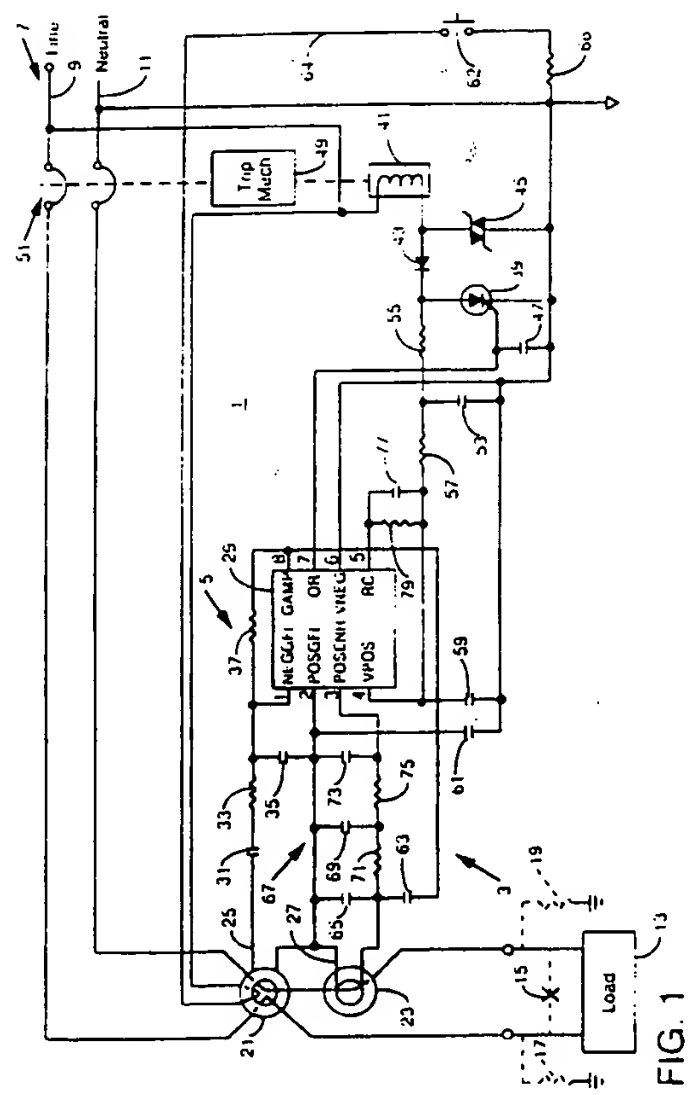

FIG. 1

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 1370

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	AU-A-628 270 (TOGAMI ELECTRIC MFG. CO.,LTD.) * page 7, paragraph 2 * * page 11; figure 5 *	1-11	H02H1/00
Y	US-A-3 801 899 (LIAO) * column 6, line 32 - line 48 *	1-11	
A	EP-A-0 313 422 (MERLIN GERIN) * column 3, line 55 - column 4, line 22; figure 1 *	1-11	
A	GB-A-2 229 053 (THE PLESSEY COMPANY) * page 4, paragraph 3 - page 5, paragraph 1; figures 1-2 *	1-11	
A	EP-A-0 094 871 (MERLIN GERIN) * page 11, line 4 - line 9; figure 2 *	1-4	
A	EP-A-0 510 795 (EATON CORPORATION) * column 23, line 41 - column 24, line 11; figures 11-14 *	1-4	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H02H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	12 July 1994	Kempen, P

EPO FORM 1503 03.82 (P04C01)

CATEGORY OF CITED DOCUMENTS

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